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Organic thin-film transistor memory with Ag floating-gate

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ABSTRACT

Organic thin-film transistor memories were realized by inserting a floating-gate layer in the Nylon 6 gate dielectrics. The transistors presented significant hysteresis behaviors and memory effect. The performance of the transistor memories, such as the memory window and the retention time, was improved greatly by using the separated silver nanoparticles instead of the silver film as the floating-gate. After the ITO source–drain electrode of the transistors treated by the oxygen plasma, the performance was further improved. The operation mechanism of the presented transistor memories was also provided and discussed.

1. Introduction

Organic electronic devices, such as organic light emitting diodes (OLED), organic solar cell, organic thin film transistors (OTFT) and organic memory devices, have been attracting increasing attention because they are promising for lightweight, flexible, large-area, and low-cost electronics. Among these organic electronic devices, OTFT memory device is an important member and become a new hot topic in both the academia and the industry, due to the potential applications like organic circuits in active-matrix OLED display [1], sensor-arrays [2], radio-frequency-identification (RFID) or smart card [3]. Up to now, the reported OTFT memory devices are mainly achieved by using ferroelectric (or ferroelectric-like) materials, such as $PbZrTiO_3$ [4], poly(vinylidenefluoridetrifluoroethylene) (PVDF/TrFE) [5–9] and nylon poly(*m*-xylylene adipamide) (MXD6) [10], as the gate dielectric layer. The direction of the polarization of the gate dielectric layer modulates the channel conductance. Actually, the transistor memory devices achieved by another way with the floating-gate embedded in the gate dielectric have been dramatic progressed in the field of silicon-based nonvolatile memory. However, there are few studies on OTFT memory devices based on the floating-gate [2,3,11–15].

In this work, we fabricated OTFT memory devices with the continuously grown silver (Ag) film and the separated silver nanoparticles (Ag-Nps) embedded in the Nylon 6 gate dielectric as the floating-gate, respectively. The performance parameters of the memory devices with the Ag-Nps floating-gate, such as the memory window and the retention time, have a prominent improvement compared with that of the memory devices with the Ag film floating gate. The memory performances can be further enhanced by treating the indium tin oxide (ITO) source–drain electrode with the oxygen plasma before the memory devices fabrication.

2. Experiment

The presented transistors were designed to be top-gate structure. Three different type memory devices with the structure cross-section schematic diagram shown in Fig. 1(a) were fabricated. The ITO coated glass slides were used as the substrate. The ITO was selectively patterned by photolithography to form the source–drain electrodes, which allowed us to select arbitrary dimension for the channel, such as in the range of $1–10^3$ μm, and to keep a very small area of the source and the drain electrodes for reducing the parasitic capacitance between the gate-source and drain. Here, the channel length/width and the ITO electrodes line width are defined as $L/W = 50$ μm/1000 μm and 50 μm, respectively. After cleaned by the routine method, the patterned substrates were put into the vacuum chamber. The pentacene film was thermally evaporated onto the substrates at a rate of about 0.8 Å/s under a pressure of 10^{-4} Pa and the resulting thickness was 60 nm. And then, the tunneling layer Nylon 6 film with a thickness of 20 nm, the floating-gate layer, and the blocking layer consisted of Nylon 6 film (230 nm) and Teflon film (150 nm) were thermally deposited in sequence. The rate of Nylon 6 and Teflon was 1 Å/s. Using the double-insulator layer of Nylon 6/Teflon to improve the performances of OTFTs has been demonstrated in

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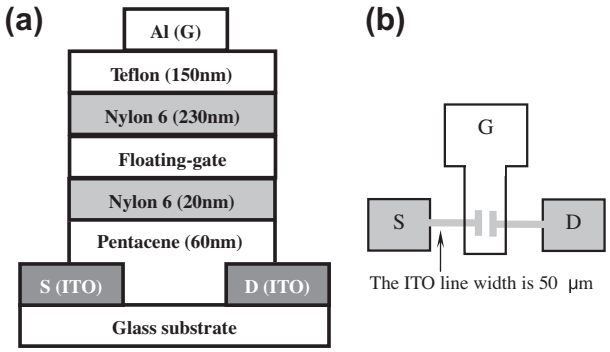

Fig. 1. (a) Cross-section schematic diagram of our organic thin-film transistor memories with Ag film or Ag-Nps as the floating-gate. (b) The plane schematic diagram of the source, drain and gate electrode.

our previous work [16]. Finally, the transistors were completed by thermal depositing 100 nm aluminum (Al) as control gate electrode with a line width of 1 mm. The plane schematic diagram of the source, drain and gate electrode is shown in Fig. 1(b). Each layer (except the ITO source/drain electrodes) was patterned by the relevant shadow mask. And the thickness of each layer can be controlled accurately by the quartz crystal thickness monitor, which is important for devices characteristics, especially for the thicknesses of the tunneling layer and the floating-gate layer. For the transistor A, 8 nm thickness Ag film was continuously grown as the floating-gate layer. The transistor B and the transistor C have a same structure, with a 15 nm thickness separated Ag-Nps as the floating-gate layer, realized by co-evaporation Ag and Nylon 6 at the rate of 0.3 and 0.7 Å/s, respectively. Before the substrate was put into the vacuum chamber, the ITO electrodes of the transistor C were treated by the oxygen plasma for 10 min, but the transistor A and B did not. The electrical characteristics of the transistors were measured using two Keithley 2400 source-measure units in dark and ambient air at room temperature.

3. Results and discussion

Fig. 2 presents the atomic force microscopy (AFM) images of the continuously grown Ag floating-gate layer and the Ag-Nps floating-gate layer, processed at the same condition with the transistor A, B and C. The continuously grown Ag forms into a successive film with a rougher surface morphology (RMS roughness of 1.69 nm), as shown in Fig. 2(a). Fig. 2(b) shows that Ag is separated to form nanoparticle islands and distribute well on the surface of the Nylon 6 film, which is agree with our initial experimental design. As estimated, the mean surface density of Ag-Nps is 5–8 $\times$ 10^8 cm^{-2} and the high of Ag-Nps is 4–12 nm.

The I_{DS}–V_{DS} characteristics of the typical floating-gate transistors at different V_G are shown in Fig. 3. The transistor A features a normal p-channel OTFT in a hole-accumulation mode with applied negative V_G. For the transistor B, the I_{DS}–V_{DS} characteristics present normal-on at V_G = 0 V and its spacing presents abnormal at the larger negative V_G, too. These two characters are more prominent for the transistor C, which are direct correlative with the memory feature of devices. Data presented in Fig. 3 are recorded when the V_G is applied from positive to negative.

The transfer characteristics (I_{DS}–V_G) of the typical floating-gate transistors are shown in Fig. 4 in the linear region with V_{DS} = −2 V. The significant anticlockwise hysteresis loops are observed when cycling V_G is applied to three transistors. And these hysteresis behaviors have no obviously change after 10 cycles, which suggest that the presented transistors have memory effect. When the V_G is larger than the threshold voltage V_T, two different phases can be defined based on the variation of the curve I_{DS}–V_G of these three type transistors. One is the conventional phase with the I_{DS} increasing linearly with the V_G. Another is the unconventional phase at more negative V_G indicated by the circle in Fig. 4.

The I_{DS} can be described in the following equation in the linear region:

$$I_{DS} = \frac{W}{L}\mu C_i\left(V_G - V_T - \frac{V_{DS}}{2}\right)V_{DS} \quad (1)$$

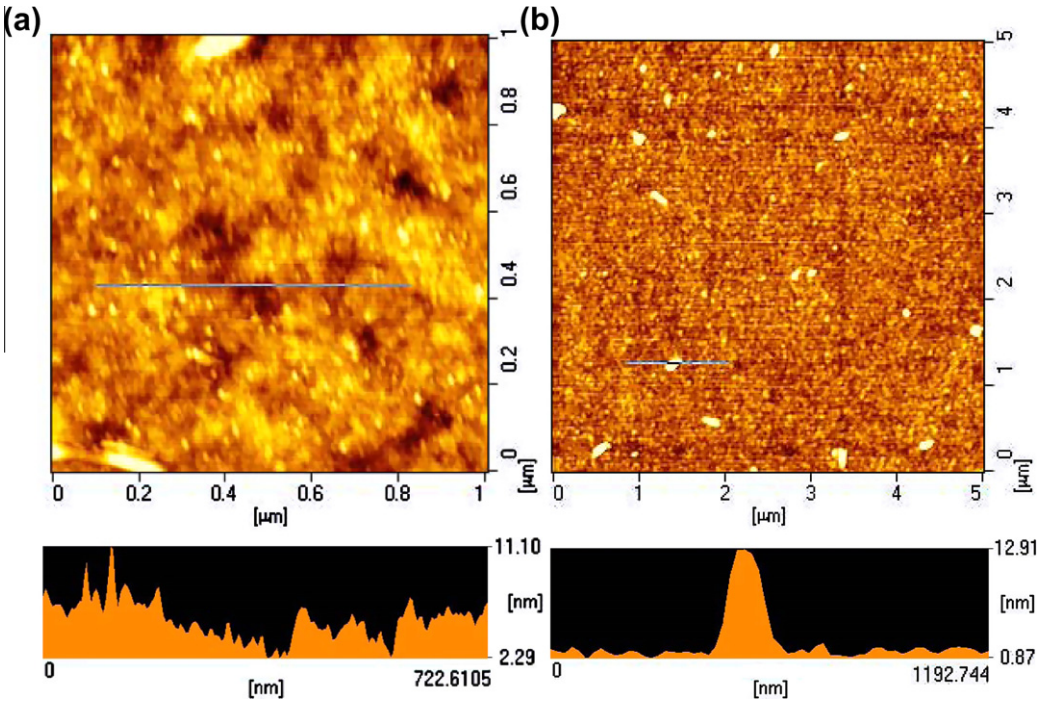

Fig. 2. The atomic force microscopy (AFM) images of the continuously grown Ag floating-gate layer (a) and the Ag-Nps floating-gate layer (b).

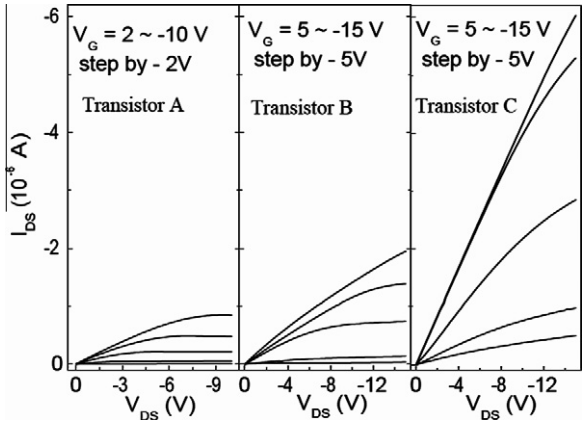

Fig. 3. The I_{DS}–V_{DS} characteristics of the OTFT memories. The data shown here are recorded with the V_G descent from positive sign to negative sign.

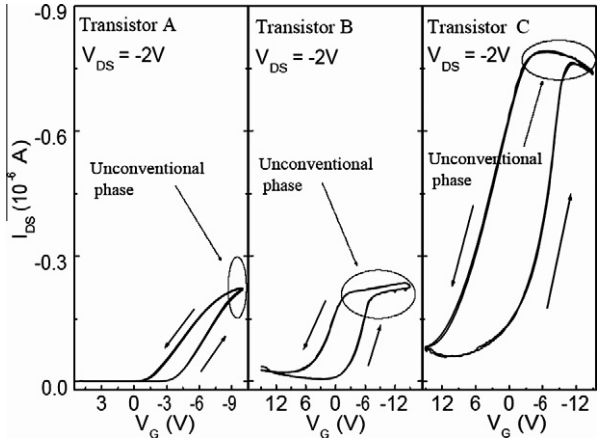

Fig. 4. The transfer characteristics of the OTFT memories. The data shown here are recorded with the V_G sweeping from positive sign to negative sign and then backtrack.

So, the field-effect mobility μ can be calculated from the following equation,

$$\mu = \frac{L}{WC_iV_{DS}}\left(\frac{\partial I_{DS}}{\partial V_G}\right)\Big|V_{DS} = const \quad (2)$$

where C_i is the gate dielectric capacitance per unit area, which can be considered as two capacitors in series with the tunneling layer and the blocking layer. That is to say the μ is directly proportional to the slope of I_{DS} versus V_G. At the conventional phase, the same mobility $\mu_{-nd} = 0.18\ cm^2/V\ s$ can be obtained for the transistor A and the transistor B at V_G swept in negative direction due to the same processing conditions leading to the same morphology of the pentacene and the Nylon 6/pentacene interface. However, the mobilities at V_G swept in positive direction have a clearly decrease, with $\mu_{-pd} = 0.15\ cm^2/V\ s$ and $0.12\ cm^2/V\ s$ for the transistor A and the transistor B, respectively (as shown in Table 1). The larger mobility of $\mu_{-nd} = 0.47\ cm^2/V\ s$ and $\mu_{-pd} = 0.24\ cm^2/V\ s$ for the transistor C are obtained, which should be ascribe to the increase of ITO work function and the enhancement of hole-injection efficiency realized by source–drain electrode treatment with the oxygen plasma [17].

The V_T for three transistors extracted from the linear region of the transfer curve I_{DS}–V_G at both V_G sweeping directions, are also shown in Table 1. The remarkably positive shift of the V_T, obtained at the V_G swept in positive direction compared with the V_G swept in negative direction, can be observed for three transistors. The memory windows (ΔV_T), signified as the shift of V_T, is one of the important performance parameters of the memory, with the value of 2.5 V, 7.5 V and 14.4 V obtained for the transistor A, B and C, respectively.

There is distinct difference for I_{DS}–V_G curves of these three transistors in the unconventional phase, with the increasing rate of the I_{DS} with the V_G decreased slightly for the transistor A, and decreased sharply for the transistor B. However, for the transistor C, the I_{DS} changes to be decreasing with the V_G. This evolution trend of the I_{DS}–V_G curve, together with the increases of the value μ_{-nd}–μ_{-pd} and the ΔV_T in the sequence of the transistor A, B and C, suggest that and the electric and memory performances of the present transistors are greatly depended on the features of the floating-gate and the source–drain electrode.

A possible explanation for the operating mechanism of present OTFT memories was provided and discussed in following. The holes, accumulated under applied negative V_G, some of them fill the traps of the pentacene/Nylon 6 and the Nylon 6 bulk, and some of them can inject into the floating-gate from the channel by the tunneling effect under enough negative V_G, and the others transport in the channel under applied V_{DS}. The memory effect is attributed to the charge storage in floating gate. In the conventional phase, the number of the transported holes increases linearly with the V_G, which result into the I_{DS} increasing linearly with the V_G. In the unconventional phase, the holes, injected into the floating-gate and filled the traps, increase with the V_G. So, the holes, transported in the channel, are not increase linearly with the V_G. The holes resided in the floating-gate can result into a build-in electric field, which also weaken the effect of the V_G on the channel. The experiment data indicate that the floating-gate with Ag-Nps can storage more holes than that with Ag film, and the increase of the ITO work function avail to the hole injection into the floating-gate, too. The increase of the holes storage in the floating-gate in sequence of transistor A, B and C, results into the different evolution trend of the I_{DS}–V_G curve in the unconventional phase, and the ΔV_T. The larger I_{DS} and the smaller mobility indicate that there are more holes transported in the channel, which can be attributed to more holes filled in the pentacene/Nylon 6 interface traps at more negative V_G, during the V_G swept at positive direction compared with that in negative direction. However, the scattering effect of the holes filled the traps result in the different of μ_{-nd} and μ_{-pd}.

The programming (P)/erasing (E) can be defined as the states with the holes injecting/rejecting the floating-gate under the applied negative/positive V_G. Thus, the reading (R) 1-state/0-state can be verified by measuring the I_{DS} upon the application reading V_G. Two storage cycles of the transistor A at $V_{DS} = -2$ V with $V_G = -10$ V/-2 V/5 V for P/R/E operation, respectively, are shown in Fig. 5a. The every operation state keeps on 25 s and the data are recorded by every 0.1 s. The transistor A shows distinct storage cycle performance. However, the I_{DS} at reading 1-state and 0-state present clear degradation. It is only 1–2 s for the ratio

Table 1
Characteristics comparison of our three different OTFT memories.

	Transistor A	Transistor B	Transistor C
$V_{T\text{-}nd}$ (V) in negative direction	−4.0	−2.5	−2.5
$V_{T\text{-}pd}$ (V) in positive direction	−1.5	5.0	11.9
ΔV_T (V)memory window	2.5	7.5	14.4
μ_{-nd} (cm^2/V s, V_G swept in negative direction)	0.18	0.18	0.47
μ_{-pd} (cm^2/V s, V_G swept in positive direction)	0.15	0.12	0.24
The retention time (s)	1–2	17	140

of $I_{DS,1\text{-}state}/I_{DS,0\text{-}state}$ (the I_{DS} at reading 1-state/the I_{DS} at reading 0-state) decreases to be 25% of the initial value. Two storage cycles of the transistor B and the transistor C at $V_{DS} = -2$ V with $V_G = -15$ V/0 V/15 V for P/R/E, are shown in Fig. 5b and c, respectively. The every operation state keeps on 5 s and the data are recorded by every 0.1 s. It can be seen that these two transistors show better storage cycle performance. The memory properties can yet keep after 100 cycles, and the currents remain repeatable without prominent degradation. It can be seen that the $I_{DS,0\text{-}state}$ show sharp degradation at initial short read time, which should be attributed to the sign instantaneous change of V_G. The lower mobility of organic semiconductor and the existence of traps at pentacene/nylon 6 interfaces should be the main reasons, leading to the slow response of holes density in the channel to V_G.For

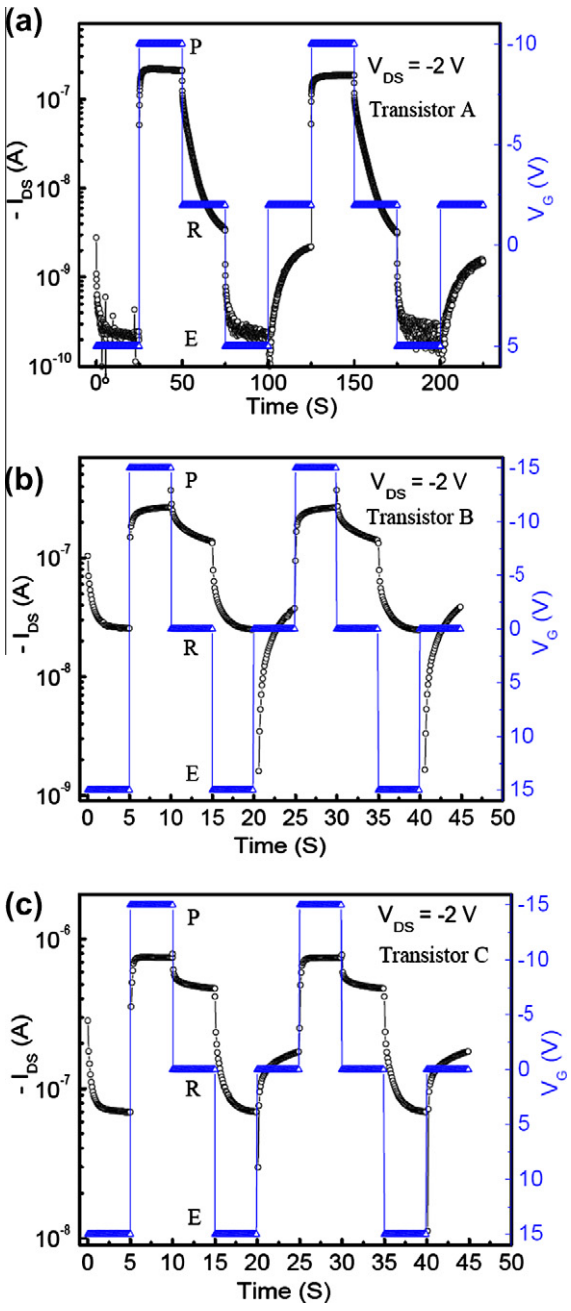

Fig. 5. Two storage cycles for: (a) transistor A with Ag film floating-gate, (b) transistor B with Ag-Nps floating-gate and (c) transistor C with Ag-Nps floating-gate and ITO source–drain electrode treated by oxygen plasma.

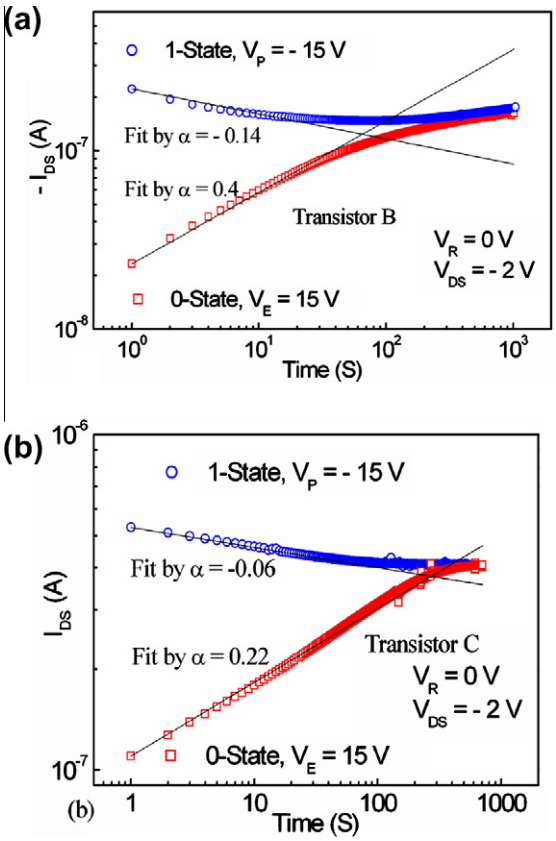

Fig. 6. The retention time of the reading 1- and 0-state for: (a) transistor B; (b) transistor C.

further describing the charge storage performance, the data retention time of the transistor B and the transistor C were measured after the P/E pulse at $V_G = -15$ V/15 V for 10 s, respectively, with the data recorded by every 1 S at $V_{DS} = -2$ V and $V_G = 0$ V, as shown in Fig. 6. The normal double logarithmic linear relation with the $I_{DS,1\text{-}state}$ and the $I_{DS,0\text{-}state}$ versus the retention time can be observed. A simulation function can be established for describing the retention time performances of the present OTFT memories, as shown in following: $I_{DS,T} = I_{DS,1} \cdot T^{\alpha}$, here, the $I_{DS,T}$ means the $I_{DS,1\text{-}state}$ or the $I_{DS,0\text{-}state}$ at the time T, $I_{DS,1}$ is the $I_{DS,1\text{-}state}$ or the $I_{DS,0\text{-}state}$ at the time $T = 1$ s, T is the retention time, α is the coefficient of the reading current degradation. The corresponding fitting results are shown in Fig. 6a and b, respectively. Smaller the absolute value of α, the $I_{DS,1\text{-}state}$ or the $I_{DS,0\text{-}state}$ is more stable. The degradation rate of the $I_{DS,1\text{-}state}$ is slower than that of the $I_{DS,0\text{-}state}$. It need about 17 s and 140 s for the ratio of the $I_{1\text{-}state}/I_{0\text{-}state}$ degrades to be 25% of the initial value in the transistor B and the transistor C, respectively. These results indicate that the transverse loss of the storage charge in the Ag film floating-gate layer is more clearly than that in the Ag-NPs floating-gate, and the treatment of ITO by oxygen plasma is beneficial the holes to inject into the deep lever of the floating-gate, which can prolong the retention time of memory.

4. Conclusions

We have successfully realized organic thin-film transistor memory by inserting the floating-gate layer of Ag film and Ag-Nps within the Nylon 6 gate dielectrics. The hysteresis and memory effects performances are attributed to charge stored in the floating-gate. The performance parameters of OTFT memories, such as the memory window and the retention time, can be improved with Ag-Nps instead of the Ag film as the floating-gate

layer due to more holes storage in the floating-gate and the decrease of the transverse loss of the storage changes in the floating-gate layer, respectively. These performance parameters can be further improved by treatment the ITO source–drain electrode with the oxygen plasma, which beneficial more holes to inject and storage in the deep lever of the floating-gate.

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